90-nm CMOS for Microwave Power Applications

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***Abstract*—We report, for the first time, the experimental evaluation of a very short channel 90-nm CMOS transistor under RF over-voltage conditions. At 9 GHz and 1.5 V supply a 40 μm gate width device is able to deliver 370 mW/mm output power with a PAE of 42% and a transducer power gain of 15 dB. Measurement results at 3 and 6 GHz is also presented. The transistor does not show any degradation in either dc or RF performance after prolonged operation at 1 and 6 dB compression. Simulation show, that the peak voltage, V_{ds} at this condition is 3.0 V, while the maximum allowed dc supply voltage is limited by the design rules to 1.2 V. We show for the first time that nanometer-scale cmos can be used for microwave power applications with severe RF over-voltage conditions without any observable degradation.**

***Index Terms*—CMOS, 90 nm, power amplifier.**

I. Introduction

THE ever-increasing market for microwave power amplifiers (PA) in wireless systems, e.g., Bluetooth, WLAN and WCDMA, requires low cost and ease of use technology which can also be integrated with other parts of the system. CMOS has been a preferred technology [1], [2] for Bluetooth and other WLAN applications. However, the low maximum voltage allowed in such technologies for reliability reasons restricts the use of CMOS for PAs. The maximum supply voltage for 90-nm CMOS is, according to [3] in the range of 1 V. Microwave PAs have per se a RF signal swinging above the supply voltage, e.g., 2 V_{ds} in a class A PA [4], which limits the allowed bias. This restriction reduces efficiency and maximum output power to a high degree. To handle the excess voltage, LDMOS transistors with increased breakdown voltage have been incorporated in CMOS processes [5], [6] at the cost of additional process complexity in custom technologies.

The scope of this paper is to show that the ordinary nanometer-scale CMOS tolerates RF over-voltage condition without degradation, thus enabling design of microwave PAs with high output power and efficiency. We do this by investigating 90-nm CMOS technology and showing results from dc and load pull measurements at 3.0, 6.0, and 9.0 GHz.

In addition, results from small signal S-parameter measurements up to 62.5 GHz are reported in Section II-B.

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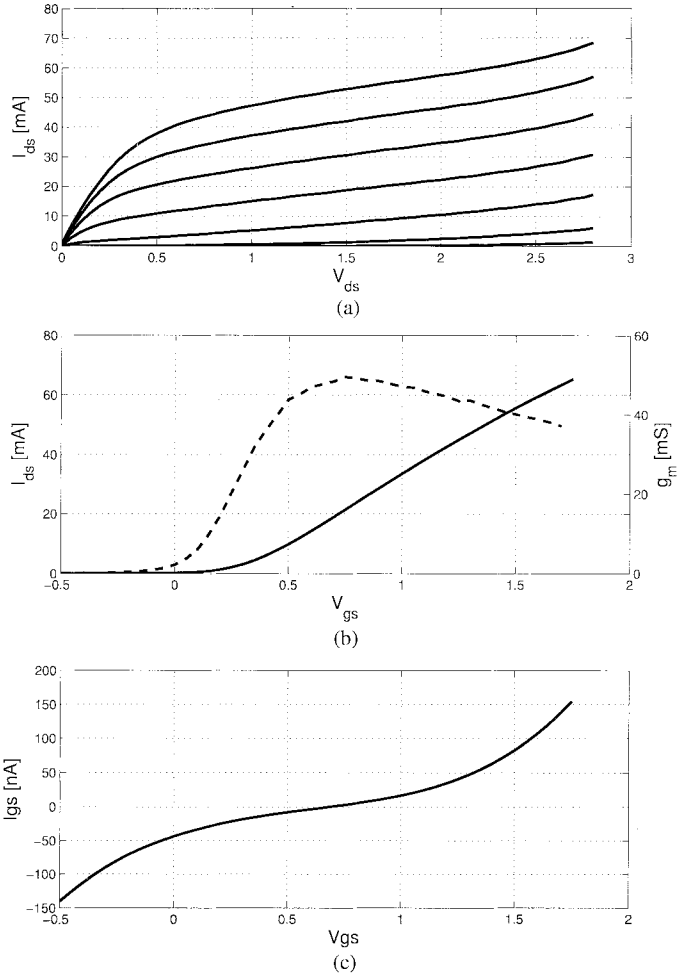

Fig. 1. (a) DC output characteristics for V_{gs} from 0 to 1.5 V in 0.25 V steps. (b) I_{ds} (solid) vs. V_{gs} and transconductance (dashed) for $V_{DS} = 1.5$ V. (c) I_{GS} for $V_{ds} = 1.5$ V.

II. Technology Description

The devices are made in a 90-nm gate length CMOS technology from IMEC, Belgium, with five metal layers of damascene Cu [7] and 1.5 nm thick gate oxide. The silicon substrate resistivity is 20 Ωcm. The maximum supply voltage is restricted by design rules to 1.2 V.

The total gate width of the CMOS transistor under investigation is 40 μm, 20 fingers with 2 μm width each.

A. DC Characteristics

The transistors were fully dc characterized using a parameter analyzer, Agilent 4156. The transconductance was calculated from the current measurement, giving $g_{m\cdot max} = 50$ mS corresponding to 1.2 S/mm as shown in Fig. 1.

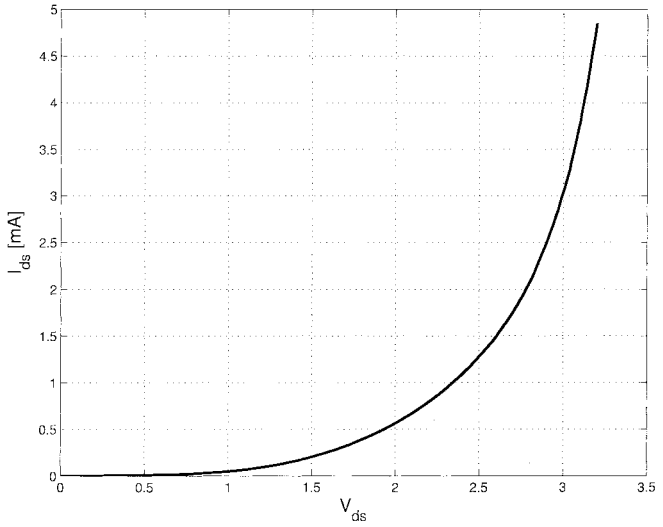

Fig. 2. Measurement of V_{ds} breakdown with $V_{gs} = 0$ V.

The drain breakdown voltage, BV_{dss} was measured to 3.2 V with $I_{ds} = 5$ mA and $V_{gs} = 0$ V. The drain current at $V_{gs} = 0$ V is substantial even at lower V_{ds} values due to the drain induced barrier lowering; see Fig. 2.

B. S-Parameter Measurements Up to 62.5 GHz

We have measured S-parameters up to 62.5 GHz with a Wiltron 360 B vector network analyzer and the device shows good frequency performance with a f_T of 140 GHz and a f_{max} of 100 GHz biased for maximum transconductance. These numbers have been extrapolated both from measurement and simulated with a nonlinear CMOS-model [8]. The main reason why f_T is higher than f_{max} is due to the large gate resistance, in comparison with HEMTs.

III. Load Pull Evaluation

Load and source pull measurement where performed, using Maury Microwave's automated load pull system, at 3.0, 6.0, and 9.0 GHz with an input power corresponding to 3 dB compression in order to match for maximum output power. The source and load where optimized for maximum output power in an iterative procedure going from source pull to load pull and vice versa to find an optimum.

The output power contours at 3 GHz with matched source is presented in Fig. 3.

With optimum load and source we reached 11.3 dBm at 6 GHz with 6 dB compression and a PAE of 43%. The device was here operating in overdriven class A. The gain and output power vs. input power as function of frequency are presented in Fig. 4. A comparison at 3, 6, 9 GHz and some competing silicon MOSFET technologies can be seen in Table I.

Our devices were stressed at both 1 dB and 6 dB compression points, at 3 and 6 GHz with dc bias $V_{gs} = 0.8$ V, $V_{ds} = 1.5$ V. The peak drain voltage was over 3 V, see IV, in the range of the breakdown voltage. We observed no degradation in neither transconductance nor gate leakage after stressing the device for 7 200 s. Neither did we see any degradation in RF performance.

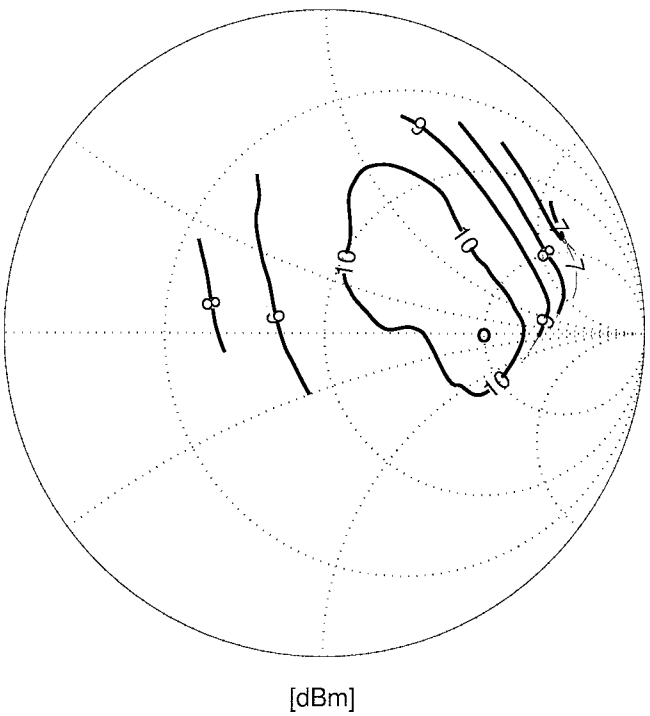

Fig. 3. Output power contours at 3 dB compression point with matched source and biased for maximum transconductance at $V_{gs} = 0.8$ V, $V_{ds} = 1.5$ V.

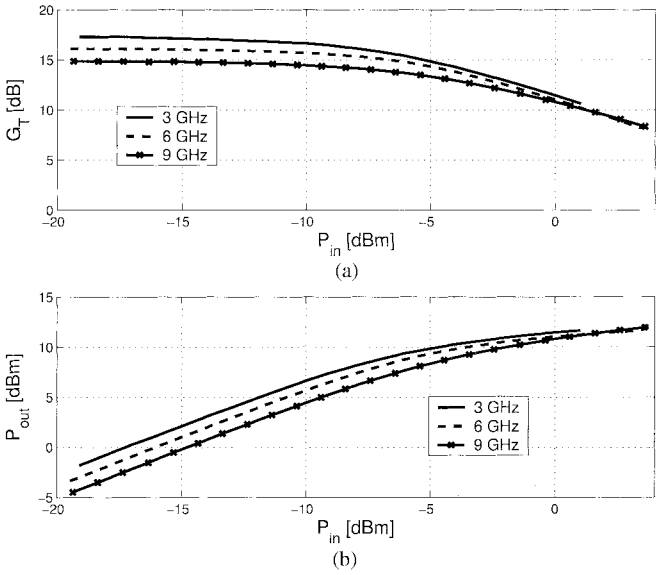

Fig. 4. (a) Transducer power gain at 3, 6, and 9 GHz. (b) Output power at 3, 6, and 9 GHz. Bias: $V_{ds} = 1.5$ V, $V_{gs} = 0.8$ V.

TABLE I
COMPARISON OF POWER PERFORMANCE. DC-BIAS: $V_{gs} = 0.8$ V, $V_{ds} = 1.5$ V (THIS WORK)

Freq. [GHz]	$G_{T,max}$ [dB]	PAE @ compression [%]	P_{out} @ compression[mW/mm]	Comment	Z_S[Ω]	Z_L [Ω]
3	17.3	43 @ 6 dB	353 @ 6 dB	This work	156+j149	115+j5
2.4	12	39 @ 4 dB	100 @ 4 dB	0.24 μm CMOS [2]	-	10+j0
5	18	62 @ 6 dB	380 @ 6 dB	0.25 μm LDMOS [7]	-	-
6	16.1	44 @ 6 dB	329 @ 6 dB	This work	187+j70	44+j26
9	14.8	42 @ 6 dB	370 @ 6 dB	This work	153+j82	34+j26

IV. Signal Simulation on Transistor Terminals

The load pull measurement offers no means to monitor the actual time domain curve forms. In order to appreciate

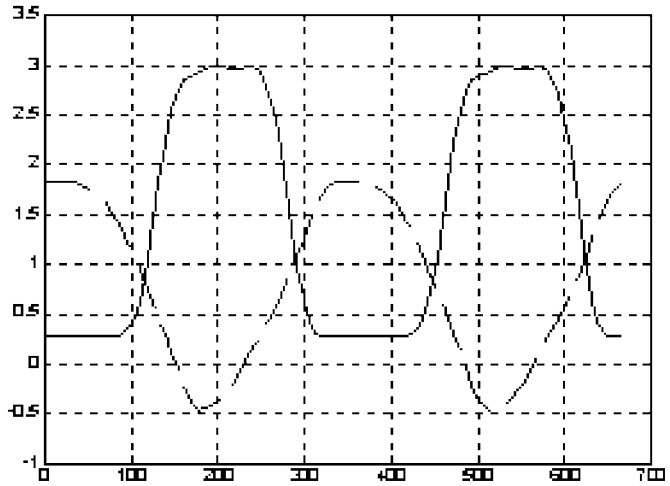

Fig. 5. Drain (solid) and gate (dashed) voltage swing for 0 dBm input power, 6 dB compression, at 3 GHz $Z_L = 115 + j5\ \Omega, Z_S = 156 + j149\ \Omega$, dc-bias: $V_{gs} = 0.8$ V, $V_{ds} = 1.5$ V.

the maximum values of V_{ds} and V_{gs} an harmonic balance simulation, with an in-house developed nonlinear model [8], was performed; see Fig. 5.

V. Discussion

Nanometer-scale CMOS transistors tolerate only very limited dc voltage, in the range of 1 V, since the high fields in the transistors cause low breakdown voltage and high leakage in the gate and drain terminals, leading to reliability problems. However, it has been shown that breakdown voltage for high frequency pulses may be higher than the dc value, at least for bipolar transistors, [9].

The prolonged stress of our devices, see III, did not result in any observable degradation of performance, suggesting that MOSFETs tolerate RF over-voltage. However, some devices degraded during dc source-drain breakdown measurements proving the deleterious influence of breakdown on reliability.

VI. Conclusion

For the first time the microwave power handling capabilities of a 90-nm CMOS transistor has been reported. The transistors show almost flat performance in output power and efficiency with frequency, while gain dropped only about 1.5 dB per GHz, a result of the very high cut off frequency.

With a supply voltage of 1.5 V, the device is capable to deliver a maximum output power, $P_{out,max} = 353,329$, and 370 mW/mm gate width at 3, 6, and 9 GHz. The mean current density is 520 mA/mm at 3 GHz and 6 dB compression. The voltage swing on the drain port has exceeded 3 V and we have not observed any degradation of device performance.

This device has also a remarkable, extrinsic, high maximum transconductance, $g_{m,max} = 1.2$ S/mm.

Acknowledgment

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